Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-13 (canceled)

Claim 14 (currently amended): An n-channel DMOS transistor source structure, comprising:

an n-type source diffusion, ohmically connected to a source metallization;

a p-type surface body diffusion which laterally surrounds at least part of said source diffusion;

a conductive gate structure which is capacitively coupled to part of said p-type surface body diffusion to define a channel region therein;

a p-type buried body diffusion which underlies said channel and said conductive gate structure and at least part of said surface body diffusion; and

an ohmic connection between said buried body diffusion and said source metallization;

whereby said buried body diffusion diverts hole current to bypass said source diffusion, and thereby reduces emission of secondary electrons, and thereby increases the safe operating area of the device.

Claim 15 (canceled)

Claim 16 (original): The structure of Claim 14, further comprising a drain region which is laterally spaced from said channel by a drift region, to thereby define a lateral DMOS transistor.

Claim 17 (previously presented): An n-channel DMOS transistor source structure, comprising:

an n-type source diffusion, ohmically connected to a source metallization;

a p-type surface body diffusion which laterally surrounds at least part of said source diffusion;

a conductive gate structure which is capacitively coupled to part of said p-type surface body diffusion to define a channel region therein;

a p-type buried body diffusion which underlies said channel and at least part of said surface body diffusion wherein said buried body diffusion is self-aligned to at least part of said source diffusion; and

an ohmic connection between said buried body diffusion and said source metallization;

whereby said buried body diffusion diverts hole current to bypass said source diffusion, and thereby reduces emission of secondary electrons, and thereby increases the safe operating area of the device.

Claim 18 (currently amended): The structure of Claim 17 ~~14~~, further comprising a drain structure which includes at least one shallow n-well diffusion laterally surrounding an n+ drain diffusion, and which is laterally spaced from said channel by a drift region, to thereby define a lateral DMOS transistor.

Claims 19-26 (canceled)

Claim 27 (withdrawn): A method for fabricating a lateral DMOS transistor, comprising:

forming a first region of a first conductivity type on a semiconductor layer;

forming a buried body region in the first region;

forming a source region of a second conductivity type opposite the first region, the source region formed such that the body is proximate the source region, and wherein a channel region is formed between an edge of the source region and an edge of the first region;

forming a drain region of a second conductivity type in the semiconductor layer, the drain region adjacent the channel region; and

forming at least one gate extending over at least a portion of the channel region.

Claim 28 (withdrawn): The method of Claim 27, wherein said action of forming a conductive body region in the first region is forming a conductive body region of the first conductivity type in the first region.

Claim 29 (withdrawn): The method of Claim 27, wherein said action of forming a conductive body region in the first region is implanting a conductive body region into the first region with a high energy implanter.

Claim 30 (withdrawn): The method of Claim 27, wherein said action of forming a conductive body region in the first region is forming a conductive body region between epitaxial layer growth steps.

Claim 31 (withdrawn): The method of Claim 27, further including the steps of:

forming one or more field oxide regions on the semiconductor layer; and

forming a gate oxide region on the first region, the channel region, and the source region,

wherein the step of forming at least one gate extending over at least a portion of the channel region is forming at least one gate upon the gate oxide region and a field oxide region.

Claim 32 (withdrawn): A product produced by the method of Claim 27.

Claim 33 (new): An n-channel DMOS transistor source structure, comprising:

an n-type source diffusion, ohmically connected to a source metallization;

a p-type surface body diffusion which laterally surrounds at least part of said source diffusion;

a conductive gate structure which is capacitively coupled to part of said p-type surface body diffusion to define a channel region therein;

a p-type buried body diffusion which underlies said conductive gate structure and at least part of said surface body diffusion; and

an ohmic connection between said buried body diffusion and said source metallization;

whereby said buried body diffusion diverts hole current to bypass said source diffusion, and thereby reduces emission of secondary electrons, and thereby increases the safe operating area of the device.

Claim 34 (new): The structure of Claim 33, further comprising a drain region which is laterally spaced from said channel by a drift region, to thereby define a lateral DMOS transistor.

Claim 35 (new): An n-channel DMOS transistor source structure, comprising:

an n-type source diffusion, ohmically connected to a source metallization;

a p-type surface body diffusion which laterally surrounds at least part of said source diffusion;

a conductive gate structure which is capacitively coupled to part of said p-type surface body diffusion to define a channel region therein;

a p-type buried body diffusion which underlies said conductive gate structure and at least part of said surface body diffusion wherein said buried body diffusion is self-aligned to at least part of said source diffusion; and

an ohmic connection between said buried body diffusion and said source metallization;

whereby said buried body diffusion diverts hole current to bypass said source diffusion, and thereby reduces emission of secondary electrons, and thereby increases the safe operating area of the device.

Claim 36 (new): The structure of Claim 35, further comprising a drain structure which includes at least one shallow n-well diffusion laterally surrounding an n+ drain diffusion,

and which is laterally spaced from said channel by a drift region, to thereby define a lateral DMOS transistor.